Rejections Under 35 U.S.C. §103

Claims 1-5, 12-16, and 23-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,289,587 to Razban (hereinafter "Razban") and further in view of U.S. Patent No. 5,862,371 to Levine et al. (hereinafter "Levine"). Applicant respectfully traverses the rejection.

Razban is directed to a method for providing a microprocessor's program counter value external to a device on a dedicated bus so that an external in-circuit emulator system can generate a list of executed instruction addresses (col. 1, lines 17-21). In-circuit emulators (or ICE systems, as are known in the art) are a combination of external software and hardware used to design and troubleshoot software programs executing on a target microprocessor or controller. Razban provides a virtual program counter value to an external ICE system via a dedicated external bus 30 (col. 4, lines 35-41, col. 4, lines 66 through col. 5, line 4). Razban eliminates the conventional requirement of monitoring system bus traffic and attempting to extract and reconstruct the instruction execution sequence (Abstract, col. 2, lines 45-57).

Levine is directed to a method and system for instruction trace reconstruction utilizing performance monitor outputs and bus monitoring (Abstract). One well known technique for reconstruction an instruction trace can be accomplished by monitoring bus traffic to determine instruction addresses, data addresses and data during the trace, if the initial architectural state of the system is known (Abstract, col. 3, lines 34-38). The difficulty in reconstructing an instruction trace from monitored bus traffic can be decreased substantially if more definitive information regarding the actual instruction sequence can be obtained (Abstract, col. 3, lines 38-41. To this end, an internal performance monitor within the processor system is utilized to generate an output each processor clock cycle which is indicative of the exact number of instructions which were executed during that clock cycle, an indication of whether or not a branch instruction was taken or not taken, an offset for each interrupt vector which has been taken, the number of data cache misses, the number of instruction cache misses, the number of store conditional instructions which were executed and the number of store conditional instructions which failed (Abstract, col. 3, lines 41-51). According to Levine, this information, in combination with monitored bus traffic may be utilized to efficiently and accurately reconstruct an instruction trace without adversely affecting performance of the system under test (Abstract, col. 3, lines 51-55). Without the necessity of actually outputting each instruction

which has been executed in a manner utilized in the prior art, the performance monitor of Levine, by outputting the above parameters, can be utilized to efficiently and accurately reconstruct an instruction trace with minimal disruption of the system under test (col. 3, lines 52-55, col. 9, lines 7-13).

Independent claim 1 recites a microcomputer comprising at least one processor, a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit, a system bus coupling the processor and debug circuit, and a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a program counter value indicating the program counter of the processor.

Applicant respectfully disagrees with the Examiner with regard to motivation for combining the references in the manner suggested. More particularly, there is no teaching or suggestion to combine the Razban and Levine references. The Examiner alleges, in paragraph three (on page 2 of the Office Action) that it "would have been obvious to one of ordinary skill at the time of the invention to include the implementation of components of the microcomputer on the same integrated circuit of Levine et al. into the system of Razban," because of one or more portions of col. 3, lines 33-51 as referenced above in the discussion of Levine. Applicant respectfully disagrees with this assertion. One skilled in the art reading Razban would not look to Levine for improvements therein. In particular, Razban teaches away from using components to monitor system bus traffic such as those taught by Levine, and it is an object of Razban to eliminate this conventional bus monitoring requirement (please see Abstract of Razban). Levine teaches an improvement of a conventional bus monitoring system (please see Abstract of Levine and col. 3, lines 33-51). One skilled in the art reading Razban would not be motivated to use elements of Levine, as Razban teaches an external monitoring that eliminates the conventional requirement of having components on-chip to monitor system bus traffic as practiced in Levine. In summary, Razban teaches away from making such a combination as suggested by the Examiner.

In view of the foregoing, the only motivation for combining the reference is found in the Applicant's application and this is improper. Because the motivation stated by the Examiner is not supported by evidence of the alleged motivation in the references, the rejection is improper and must be withdrawn. See *In re Dembiczak 175 F.3d 994, 50 U.S.P.Q.2d*

(BNA) 1614 (Fed. Cir. 1999). ("Combining prior art references without *evidence* of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight." [emphasis added])

Further, even if the references were combined as suggested by the Examiner, claim 1 distinguishes over the combination. In particular, the references, when combined, do not teach or suggest a "processor and debug circuit [that] are implemented on a same integrated circuit" and "a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a program counter value indicating the program counter of the processor," as recited in claim 1.

As discussed in the previous amendment, Razban does not transmit the program counter to a debug circuit located on an integrated circuit; Razban only transmits the program counter off-chip to an external system. Levine does not supply the missing limitation, as Levine merely monitors output instructions and their addresses as they are moved into the processor on the bus, the number of instructions executed during each clock cycle, the occurrence of interrupts, and whether branch conditional constructions were taken or not taken (Abstract, col. 8, line 59 - col. 9, line 13). Levine does not transmit a value of the program counter from the processor to a debug circuit located on a same integrated circuit. Levine clearly indicates that the above parameters (and only the above parameters) are needed to reconstruct instruction trace. Levine does not indicate obtaining a value of the program counter and transmitting it to an on-chip debug circuit. Therefore, even if combined, claim 1 distinguishes over the combination. Thus, the combination is first improper, and second, the combination does not render obvious claim 1. Therefore, the rejection should be withdrawn. Claims 2-9 and 11 depend from claim 1 and are allowable for at least the same reasons.

Independent Claim 12

Independent claim 12 recites a microcomputer comprising at least one processor, a debug circuit, a system bus coupling the processor and the debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit, and means for transmitting to the debug circuit a program counter value indicating the program counter of the processor.

As discussed above, with reference to claim 1, the combination of Razban and Levine is improper. Further, even if the references are combined in the manner suggested, claim 12 patentable distinguishes over the combination. In particular, neither reference teaches or suggests a processor and a debug circuit, "wherein the processor and debug circuit are implemented on a same integrated circuit" and "means for transmitting to the debug circuit a program counter value indicating the program counter value of the processor," as recited in claim 12. As discussed above with reference to claim 1, neither Razban nor Levine teaches or suggests transmitting a program counter value to a debug circuit from a processor located on a same integrated circuit. Therefore, the combination of cited references is first, improper, and second, claim 12 distinguishes over the combination. Therefore, the rejection of claim 12 should be withdrawn. Claims 13-20 and 22 depend from claim 12 and are allowable for at least the same reasons.

Independent Claim 23

Independent claim 23 recites a method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of transmitting, to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor.

As discussed above with reference to claim 1, the combination of Razban and Levine is improper. Further, even if the references are combined in the manner suggested, claim 23 distinguishes over the combination. In particular, neither reference teaches or suggests a "processor and debug circuit being implemented on a same integrated circuit" and "transmitting, to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor" as recited in claim 23. As discussed above with reference to claim 1, neither Razban nor Levine teaches or suggests transmitting a program counter value on a communication link coupling the processor and debug circuit, the processor and debug circuit being implemented on a same integrated circuit. Therefore, the combination of the cited references is first, improper, and second, claim 23 distinguishes over the combination. Therefore, the rejection of claim 23 should be withdrawn. Claims 24-33 depend from claim 23 and are allowable for at least the same reasons.

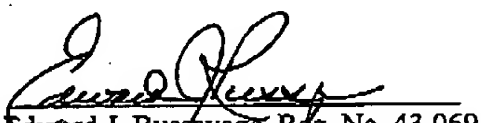
CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

David A. Edwards et al., Applicant

By: 

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